

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 4

Complete if Known

Application Number	10/648,434
Filing Date	August 27, 2003
First Named Inventor	Sanjay DABRAL
Group Art Unit	2822
Examiner Name	Not Yet Assigned
Attorney Docket Number	2207/597504

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
JZ		US- 5,461,338	10-24-95	Hirayama et al.	
JZ		US- 5,557,231	09-17-96	Yamaguchi et al.	
JZ		US- 5,559,368	09-24-96	Hu et al.	
JZ		US- 5,689,144	11-18-97	Williams	
JZ		US- 5,689,209	11-18-97	Williams et al.	
JZ		US- 6,493,430	12-10-02	Leuca et al.	
JZ		US- 6,100,751	08-08-00	De et al.	
JZ		US- 6,218,895	04-17-01	De et al.	
JZ		US- 6,300,819	10-09-01	De et al.	
JZ		US- 6,166,584	12-26-00	De et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
JZ		WO 98/59419	16 JUNE 1998	DE et al.		

Examiner
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Jeffrey Zweizig

Date
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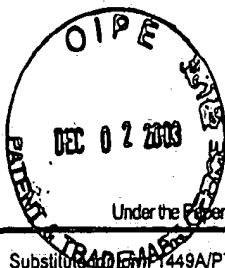
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Substituted Form PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/648,434
		Filing Date	August 27, 2003
		First Named Inventor	Sanjay DABRAL et al.
		Group Art Unit	2822
		Examiner Name	TO BE ASSIGNED
Sheet 2 of 4	Attorney Docket Number	2207/597504	

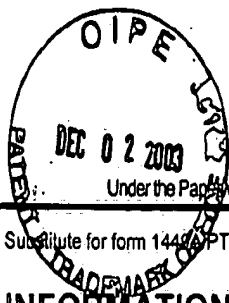
OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JZ		Excerpt from "1996 IEEE International SOI Conference Proceedings" (October 1996) p. 141.	
JZ		ANTONIADIS, D.A. and CHUNG, J.E., "Physics And Technology Of Ultra Short Channel MOSFET Devices", <i>IEDM Technical Digest</i> (1991) pp. 2.1.1 - 2.1.4.	
JZ		AOKI, M. et al., "0.1 μ m CMOS Devices Using Low-Impurity-Channel Transistors (LICT)", <i>IEDC Technical Digest</i> , (1990) pp. 9.8.1-9.8.3.	
JZ		ASSADERAGHI, F. et al., "High-Performance Sub-Quarter-Micrometer PMOSFET's on SOI", <i>IEEE Electron Device Letters</i> , Vol. 14, No. 6 (June 1993) pp. 298-300.	
JZ		ASSADERAGHI, F. et al., "A Dynamic Threshold Voltage MOSFET (DTMOS) For Ultra-Low Voltage Operation", <i>IEDM Technical Digest</i> , (1994) pp. 33.1.1-33.1.4.	
JZ		KIOI, K. et al., "Forward Body-Bias SRAM Circuitry On Bulk Si With Twin Double-Well", <i>Electronics Letters</i> , Vol. 33, No. 23 (November 1997) pp. 1929-1930.	
JZ		KIOI, K. et al., "Forward Body-Bias MOS (FBMOS) Dual Rail Logic Using An Adiabatic Charging Technique With Sub-0.6V Operation" <i>Electronics Letters</i> , Vol. 33, No. 14 (July 1997) pp. 1200-1201.	
JZ		DeCHIARO, L.F. and SANDROFF, C.J., "Improvements In Electrostatic Discharge Performance of InGaAsP Semiconductor Lasers By Facet Passivation" <i>IEEE Transactions On Electron Devices</i> , Vol. 39, No. 3 (March 1992) pp. 561-565.	
JZ		KOTAKI, H. et al., "Novel Bulk Dynamic Threshold Voltage MOSFET (B-DTMOS) With Advanced Isolation (SITOS) And Gate To Shallow-Well Contact (SSS-C) Processes For Ultra Low Power Dual Gate (CMOS)", <i>IEDM Technical Digest</i> 96-459 (1996) pp. 17.7.1-17.7.2, 17.7.4.	
JZ		KAWAGUCHI, H. et al., "A CMOS Scheme For 0.5 V Supply Voltage With Pico-Ampere Standby Current", <i>IEEE International Solid-State Circuits Conference, Session 12/TD: Low-Voltage and Multi-Level Techniques</i> , Paper FP 12.4, (1998) pp. 192-193.	
JZ		KURODA, T. and SAKURAI, T., "Threshold-Voltage Control Schemes Through Substrate-Bias For Low-Power High-Speed CMOS LSI Design", <i>Journal OF VLSI Signal Processing Systems</i> 13, (1996) pp. 107-117.	
JZ		KURODA, T. et al., "Substrate Noise Influence On Circuit Performance In Variable Threshold-Voltage Scheme", <i>International Symposium On Low Power Electronics And Design</i> , (August 1996) pp. 309-312.	
JZ		KURODA, T. et al., "Variable Supply-Voltage Scheme For Low-Power High-Speed CMOS Digital Design", <i>IEEE Journal Of Solid-State Circuits</i> , Vol. 33, No. 3 (March 1998) pp. 454-462.	

Examiner Signature	Jeffrey Zweig	Date Considered	5/25/04
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Substitute for form 1442 PTO

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Application Number	10/648,434
Filing Date	August 27, 2003
First Named Inventor	Sanjay DABRAL et al.
Group Art Unit	2822
Examiner Name	TO BE ASSIGNED
Attorney Docket Number	2207/597504

Sheet 3 of 4

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
JZ		KURODA, T. et al., "A 0.9-V, 150-MHz, 10-mW, 4mm ² , 2-D Discrete Cosine Transform Core Processor With Variable Threshold-Voltage (VT) Scheme", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 31, No. 11 (November 1996) pp. 1770-1779.	
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JZ		RODDER, M. et al., "A Sub-0.18 μ m Gate Length CMOS Technology For High Performance (1.5V) And Low Power (1.0V)", <i>IEDM Technical Digest</i> 96-563 (1996) pp. 563-566.	
JZ		ROFALL, S. and Y. SENG, "Experimentally-Based Analytical Model Of Deep-Submicron LDD pMOSFET's In A Bi-MOS Hybrid-Mode Environment", <i>IEEE Transactions On Electron Device</i> , Vol. 44, No. 9 (September 1997) pp. 1473-1482.	
JZ		SAKURAI, T. et al., "Low-Power CMOS Design through V _{TH} Control and Low-Swing Circuits", <i>International Symposium On Low Power Electronics And Design</i> , (August 1997) pp. 1-6.	
JZ		SPLAIN, C. and KENNETH, K.O., "Ultra Low Voltage Complementary Metal Oxide Semiconductor (ULV-CMOS) Circuits: Bulk CMOS Operation Below Threshold (V _{TO})", <i>IEEE Southeastcon '96 - Bringing Together Education, Science And Technology</i> , (1996) pp. 670-673.	
JZ		STREETMAN, B., "Section 8.3 The Metal-Insulator-Semiconductor Fel", <i>Solid State Electronic Devices</i> , 2nd Edition, Library of Congress, (1980) pp. 317-319.	
JZ		THOMPSON, S. et al., "Dual Threshold Voltages And Substrate Bias: Keys To High Performance, Low Power, 0.1 μ m Logic Designs, <i>Symposium On VLSI Technology Design Of Technical Papers</i> , (1997) pp. 69-70.	
JZ		WONG, Louis S.Y. et al., "SA 17.4: A 1V CMOS Digital Circuits with Double-Gate-Driven MOSFET", <i>ISSCC97/SESSION 17/ID: LOW-POWER/LOW-VOLTAGE CIRCUITS/PAPER SA 17.4, Digest of Technical Papers</i> .	

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Signature

Jeffrey Zweizig

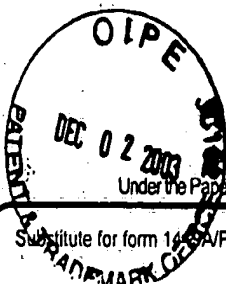
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Sheet 4 of 4

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JZ		WALKER, W. et al., "Design And Analysis Of A CMOS SOS/SOI Receiver For A Radiation Hard Computer", <i>IEEE SOS/SOI Technology Conference</i> , (October 1989) pp. 167-168.	
JZ		WANN, H. Clement et al., "Channel Doping Engineering Of MOSFET With Adaptable Threshold Voltage Using Body Effect For Low Voltage And Low Power Applications", <i>International Symposium On VLSI Technology, Systems and Applications - Proceedings Of Technical Papers</i> , (1995) pp. 159-163.	
JZ		"WANN, Clement H. et al., "A Comparative Study of Advanced MOSFET Concepts", <i>IEEE Transactions On Electron Devices</i> , Vol. 43, No. 10, (October 1996) pp. 1742-1751.	
JZ		WILLIAMS, R. et al., "MOSFET Flyback-Diode Conduction and dV/dt Effects in Power ICs in Low-Voltage Motor Control Applications", <i>Proceedings of the 3rd International Symposium on Power Semiconductor Devices and ICs</i> , (June 1991), pp. 254-257.	

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